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REMARKS

The indication of allowable subject matter in claims 10-12 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 7-8 stand rejected under 35 U.S.C. § 102 as being anticipated by Miyashita et al. '828 ("Miyashita"). Claim 7 is independent. This rejection is respectfully traversed for the following reasons.

In order to expedite prosecution, Applicants' representative initiated a telephone interview with Examiner Ghulamali. Applicants and Applicants' representative would like to thank Examiner Ghulamali for his courtesy in conducting the interview and for his assistance in resolving issues. As a result of the interview, Examiner Ghulamali indicated that he understood and appreciated the asserted distinctions between claims 7-8 and Miyashita, and would reconsider his position upon receiving a formal response. A summary of the interview discussion follows.

Claim 7 recites in pertinent part, "a first phase detector for detecting a phase error in the clock with respect to ***one*** of a rising edge and a falling edge of the data signal ...; a second phase detector for detecting a phase error in the clock with respect to the ***other one*** of the rising edge and the falling edge of the data signal ...; and means for controlling a transition characteristic of ***the data signal according to an output of one of the first and second phase detectors***" (emphasis added). As discussed during the interview, Miyashita is completely silent as to a first and second phase detector which detect phase error with respect to the rising and falling edge of the data signal, ***respectively***. In contrast, as shown in Figure 7 of Miyashita, only one phase detector 20 is described; and the phase detectors in the ***distinct*** embodiment shown in Figures

89-90 of Miyashita each function, at best, similarly to the phase detector of the Figure 7 embodiment in that the phase error is detected across the entire transition cycle of a given signal.

Moreover, as further discussed during the interview, Miyashita fails to disclose or suggest "a means for controlling a transition characteristic of the data signal according to an output of one of the first and second phase detectors." As shown in Figure 7 of Applicants' drawings, in one exemplary embodiment of the present invention, the exemplary control signal DCONT from the output of PD 113 can be fed back to, for example, a receiver 101 (*see, e.g.,* page 12, lines 3-7 of Applicants' specification) for effecting control of a transition characteristic of the ***data signal*** (as opposed to the clocks) inputted into the receiver 101. Miyashita does not disclose or suggest control of a transition characteristic of the data signal itself, let alone according to a phase detector output. In contrast, as shown in Figure 7 of Miyashita, the output of the single phase detector 20 is used to synchronous the respective clock phases and is simply supplied to the VCO 50 for controlling ***clock*** transitions. Indeed, the data signal of Miyashita is inputted directly into the phase detector 20 without any means by which the data signal transition characteristic can be controlled, let alone according to an output of phase detector 20 which is instead used to control the VCO clocks.

As noted on page 10, lines 12-20 of Applicants' specification, one of the objects of the present invention is to enable the data transition characteristic of a driver or receiver to be adjusted ***before entering the actual data transfer period,*** thereby providing the capability to suppress a timing jitter in the recovered clock. Miyashita is silent as to this effect, let alone suggest a means by which to realize such an effect, and therefore has no disclosed need or desire for a means for controlling a transition characteristic of the data signal according to an output of a phase detector (let alone for a first and second phase detector which detect phase error with

respect to the rising and falling edge of the data signal, ***respectively***.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that Miyashita does not anticipate claim 7, nor any claim dependent thereon.

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 7 is patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination.

Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejection under 35 U.S.C. § 102 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's

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amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

Ramyar M. Farid
Registration No. 46,692

600 13th Street, N.W.
Washington, DC 20005-3096
Phone: 202.756.8000 RMF:MWE
Facsimile: 202.756.8087
Date: April 18, 2006

Please recognize our Customer No. 20277 as our correspondence address.